Quick Guide of Jumper Setting and operation of FBs-7SG Module

This guide is a supplement mainly for the users who have used the FBe-7SG module. Before the formal FBs user's manual is complete, for those users who never used the FBe-7SG module, please also refer the content of FBE Advance manual chapter 17.

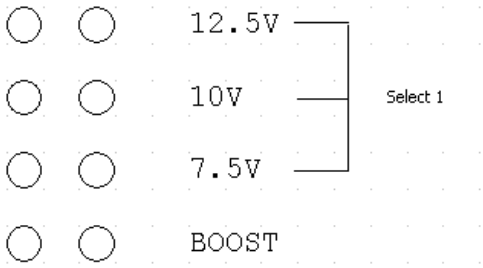
1. Jumpers function and its location

	Jumper	Location	Function
Common Control	**JP2**	Lower position	Decode(With jumper)/non-decode(No jumper)
	JP3	Lower position	O.V. test(T)or normal(N)
	JP1	Rear side	High driving voltage selection
DISP0	**JP5**	Upper position	High(HV)/Low(LV) driving voltage selection *1
	JP6	Upper position	0.6V(0.6V) voltage drop selection
	JP7	Upper position	1.2V(1V2) voltage drop selection
DISP1	**JP8**	Lower position	High(HV)/Low(LV) driving voltage selection *1
	JP9	Lower position	0.6V(0.6V) voltage drop selection
	JP10	Lower position	1.2V(1V2) voltage drop selection

Note 1: High(HV)/Low(LV) driving voltage selection jumper must be inserted with short metal bar horizontally.

2. High driving voltage selection – JP1

This jumper is located at the rear side of the module, please turn the module's bottom face up when perform the setting.



The upper three jumpers can only be selected one for shorted when usage. This setting only takes effective when the High(HV)/Low(LV) driving voltage selection jumper is set to HV position. When the jumper is positioned at LV, the driving voltage is 5V.

When BOOST jumper is shorted, the driving voltage will be boosted about 5% from its nominal value can be used for compensation of line voltage drop.

3. I/O address occupation and displays

Module	Display Mode	I/O Occupied	Model ID.	Displays
7SG1	Decode	3 R.O.	7SG1S	8 Digits
	Non-Decode	4 R.O.	7SG1H	64 Segments
7SG2	Decode	5 R.O.	7SG2S	16 Digits
	Non-Decode	8 R.O.	7SG2H	128 Segments

4. Display control

The pattern of the LED display driven by the FBs-7SG LED display control module can be easily controlled by fill up the contents of the corresponding output registers. For more complicate applications, e.g. leading zero display control, message scrolling and 16-segment display control, we provide a handy instruction TDSP to facilitate the user's coding. Please refer the User's manual for detail description of TDSP.

Display control of 7SG1 - decode mode

The **Rm** at following table represent the first output register allocated for 7SG1 module

Rm+0	This register controls the decimal point display of every digit. D7~D0 control the decimal point of 8^{th}~ 1^{st} digit respectively. The decimal point will be lighted when the corresponding control bit is 1.
Rm+1	This register controls the display of 4^{th}~ 1^{st} digit. Every 4 bits(nibble) control one digit. D3~D0 control the first digit(right most), D7~D4 control the second digit, D11~D8 control the third digit while D15~D12 control the fourth digit.
Rm+2	This register can control the display of 8^{th}~ 5^{th} digit. Every 4 bits(nibble) control one digit. D3~D0 control the 5^{th} digit, D7~D4 control the 6^{th} digit, D11~D8 control the 7^{th} digit while D15~D12 control the 8^{th} digit(left most).

Please refer the contents of page 4 for the corresponding decoded display patterns for each 4 bits combination value.

Display control of 7SG1 - non-decode mode

The **Rm** at following table represent the first output register allocated for 7SG1 module

Rm+0	This register controls the segment display of 2^{nd}~ 1^{st} digit. Every 8 bits(byte) control one digit. D7~D0 control the first digit(right most), D15~D8 control the second digit.
Rm+1	This register controls the segment display of 4^{th}~ 3^{rd} digit. Every 8 bits(byte) control one digit. D7~D0 control the 3^{rd} digit, D15~D8 control the 4^{th} digit.
Rm+2	This register controls the segment display of 6^{th}~ 5^{th} digit. Every 8 bits(byte) control one digit. D7~D0 control the 5^{th} digit, D15~D8 control the 6^{th} digit.
Rm+3	This register controls the segment display of 8^{th}~ 7^{th} digit. Every 8 bits(byte) control one digit. D7~D0 control the 7^{th} digit, D15~D8 control the 8^{th} digit(left most).

Please refer the contents of page 5 for the corresponding driven segment for each control bits.

Display control of 7SG2 - decode mode

The **Rm** at following table represent the first output register allocated for 7SG2 module

Rm+0	This register controls the decimal point display of every digit. D15~D0 control the decimal point of 16th~ 1st digit respectively. The decimal point will be lighted when the corresponding control bit is 1.
Rm+1	This register controls the display of 4th~ 1st digit. Every 4 bits(nibble) control one digit. D3~D0 control the first digit(right most), D7~D4 control the second digit, D11~D8 control the third digit while D15~D12 control the fourth digit.
Rm+2	This register controls the display of 8th~ 5th digit. Every 4 bits(nibble) control one digit. D3~D0 control the first digit, D7~D4 control the second digit, D11~D8 control the third digit while D15~D12 control the fourth digit.
Rm+3	This register controls the display of 12th~ 9th digit. Every 4 bits(nibble) control one digit. D3~D0 control the 9th digit, D7~D4 control the 10th digit, D11~D8 control the 11th digit while D15~D12 control the 12th digit.
Rm+4	This register can control the display of 16th~ 13th digit. Every 4 bits(nibble) control one digit. D3~D0 control the 13th digit, D7~D4 control the 14th digit, D11~D8 control the15th digit while D15~D12 control the 16th digit(left most).

Please refer the contents of page 4 for the corresponding decoded display patterns for each 4 bits value

Display control of 7SG2 - non-decode mode

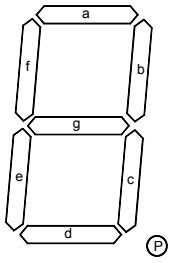
The **Rm** at following table represent the first output register allocated for 7SG2 module

Rm+0	This register controls the segment display of 2nd~ 1st digit. Every 8 bits(byte) control one digit. D7~D0 control the first digit(right most), D15~D8 control the second digit.
Rm+1	This register controls the segment display of 4th~ 3rd digit. Every 8 bits(byte) control one digit. D7~D0 control the 3rd digit, D15~D8 control the 4th digit.
Rm+2	This register controls the segment display of 6th~ 5th digit. Every 8 bits(byte) control one digit. D7~D0 control the 5th digit, D15~D8 control the 6th digit.
Rm+3	This register controls the segment display of 8th~ 7th digit. Every 8 bits(byte) control one digit. D7~D0 control the 7th digit, D15~D8 control the 8th digit.
Rm+4	This register controls the segment display of 10th~ 9th digit. Every 8 bits(byte) control one digit. D7~D0 control the 9th digit, D15~D8 control the 10th digit.
Rm+5	This register controls the segment display of12th~ 11th digit. Every 8 bits(byte) control one digit. D7~D0 control the 11th digit, D15~D8 control the 12th digit.

Rm+6	This register controls the segment display of 14th~ 13th digit. Every 8 bits(byte) control one digit. D7~D0 control the 13th digit, D15~D8 control the 14th digit.
Rm+7	This register controls the segment display of 16th~ 15th digit. Every 8 bits(byte) control one digit. D7~D0 control the 15th digit, D15~D8 control the 16th digit(left most).

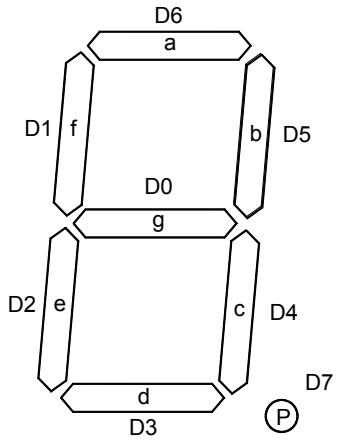
Please refer the contents of page 5 for the corresponding driven segment for each control bits.

Display pattern for decoded mode

Nibble value		Segment designation	Segment data							Display pattern
Hexade cimal	Binary		a	b	c	d	e	f	g	
0	0000		1	1	1	1	1	1	0	
1	0001		0	1	1	0	0	0	0	
2	0010		1	1	0	1	1	0	1	
3	0011		1	1	1	1	0	0	1	
4	0100		0	1	1	0	0	1	1	
5	0101		1	0	1	1	0	1	1	
6	0110		1	0	1	1	1	1	1	
7	0111		1	1	1	0	0	1	0	
8	1000		1	1	1	1	1	1	1	
9	1001		1	1	1	1	0	1	1	
A	1010		0	0	0	0	0	0	1	
B	1011		1	0	0	1	1	1	1	
C	1100		0	1	1	0	1	1	1	
D	1101		0	0	0	1	1	0	1	
E	1110		0	0	0	1	1	1	1	
F	1111		0	0	0	0	0	0	0	

Following segment designation only apply for the LED display board provided by FATEK.

Non-decode mode bit control designation for seven-segment display device



Non-decode mode bit control designation for 16-segment display device